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SITE-SPECIFIC METHODOLOGY FOR LOCALIZATION AND ANALYZING JUNCTION DEFECTS IN MOSFET DEVICES

Abstract

This invention relates to a method for electrically localizing site-specific defective sub 130nm node MOSFET devices with shallow (less than 80nm deep) source/drain junctions utilizing bulk silicon, or Silicon on Insulator (SOI), or strained silicon (SE), followed by optimized sample preparation steps that permits imaging, preferably high resolution electron holographic imaging, in an electron microscope to detect blocked implants, asymmetric doping, or channel length variations affecting MOSFET device performance. Detection of such defects in such shallow junctions enables further refinements in process simulation models and permits optimization of MOSFET device designs.